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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/730,780	PORTERFIELD, A. KENT	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the After Final Amendment filed on 10th of May 2004. Claims 1, 10, 19, 28, 34, 45, 51, 57 and 59 have been amended; claim 60 has been canceled; and no claim has been newly added since the Final Office Action was mailed on 9th of February 2004.

2. Receipt is acknowledged of the request filed on 29th of June 2004 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/730,780, which the request is acceptable and an RCE has been established. Currently, claims 1-59 are pending in this application.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 2, 16-20, 34, 35, 38-40, 51, 52, 55-57 and 59 are rejected under 35 U.S.C. 102(e) as being anticipated by Ajanovic et al. [US 6,539,444 B1; hereinafter Ajanovic].

Referring to claims 1 and 34, Ajanovic discloses a bus arbitration method (See Fig. 2 and col. 3, line 65 through col. 4, line 26) for a processor based system (i.e., system 100 of Fig. 1; See Fig. 1 and col. 2, lines 50-60), said system comprising a hub device, which is a link hub (i.e., MCH 120 of Fig. 1) for a link bus (i.e., hub interfaces A, B, C and D in Fig. 1) comprising a plurality of link bus segments (i.e., HI A, HI B, HI C and HI D in Fig. 1), said hub device coupled to a processor (i.e., MCH 120 coupled to processors 102, 104, 106 and 108 in Fig. 1) by a processor bus (i.e., processor bus 110 of Fig. 1) and coupled to a memory device (i.e., main memory 123 of Fig. 1) by a memory bus (i.e., bus between memory interface 122 and main memory 123 in Fig. 1), said hub device being connected to a first device,

which is a satellite device (e.g., bus agents Bridge 127 or ICH 140 in Fig. 1) by one of said link bus segments (i.e., one of hub interfaces HI A, HI B, HI C and HI D in Fig. 1), said method comprising the steps of issuing, from one of said first device and said hub device (i.e., one of said bus agents), an arbitration request (i.e., ARBITRATION 202 and REQUEST 204 in Fig. 2) on said link bus (See col. 4, lines 1-6); determining, at said first device and said hub device, whether control of said link bus can be transferred from a bus master (i.e., hub agent A in Fig. 13) to said device (i.e., hub agent B in Fig. 13) issuing said arbitration request (i.e., requesting ownership of hub interface; See col. 9, lines 48-50); and if it is determined that control of said link bus can be transferred (See col. 9, lines 52-54), transferring control of said link bus from said bus master to said device issuing said arbitration request (i.e., releasing hub agent A's ownership; See step 1310 in Fig. 13 and col. 9, lines 60-61), wherein control of said link bus is granted by said first device and said hub device (See Figs. 11-13; i.e., wherein in fact that hub agent A releases hub interface to hub agent B in Fig. 13, step 1310, inherently anticipates that control of link bus is granted by said first device and said hub device).

Referring to claims 2 and 35, Ajanovic teaches said first device and said hub device (i.e., bus agents in Fig. 1) performs the steps of inspecting (i.e., sampling) internal arbitration state (i.e., state of hub agent) and status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16); and determining if control of said link bus can be transferred (See col. 9, lines 48-50) based on said inspected (i.e., sampled) internal arbitration state and status information (See Figs. 11 and 12; i.e., based on state of hub agent if it is active or inactive; See col. 9, lines 12-16 and 34-38).

Referring to claims 16, 17, 39 and 40, Ajanovic teaches said link bus (i.e., hub interfaces A, B, C and D in Fig. 1) comprising a link bus status line (i.e., RQA and RQB in Fig. 14) and said arbitration request arbitration request, i.e., an arbitration request signal (i.e., ARBITRATION 202 and REQUEST 204 in Fig. 2), is issued by propagating a signal (i.e., transmitting active or inactive signal; See col. 9,

lines 12-16 and 34-38) on said link bus status line in time-multiplexing (See col. 8, line 56 through col. 9, line 4).

Referring to claim 18, Ajanovic teaches said issuing step through said transferring step are performed in accordance with a link bus protocol (i.e., PROTOCOL LAYER) of said link bus (See col. 5, line 65 through col. 6, line 23).

Referring to claim 19, Ajanovic discloses a method of arbitrating control (See Fig. 2 and col. 3, line 65 through col. 4, line 26) of a link bus (i.e., hub interfaces A, B, C and D in Fig. 1) comprising a plurality of link bus segments (i.e., HI A, HI B, HI C and HI D in Fig. 1) in a computer system (i.e., system 100 in Fig. 1; See col. 2, lines 50-60), said computer system comprising a hub device (i.e., MCH 120 of Fig. 1) for said plurality of link bus segments, said hub device coupled to a processor (i.e., MCH 120 coupled to processors 102, 104, 106 and 108 in Fig. 1) by a processor bus (i.e., processor bus 110 of Fig. 1) and coupled to a memory device (i.e., main memory 123 of Fig. 1) by a memory bus (i.e., bus between memory interface 122 and main memory 123 in Fig. 1), said hub device being connected to a satellite device (e.g., bus agents Bridge 127 or ICH 140 in Fig. 1) by one of said link bus segments (i.e., one of hub interfaces HI A, HI B, HI C and HI D in Fig. 1), said link bus being a source strobed bus (i.e., hub interface with source synchronous clock mode; See col. 4, lines 35-38 and col. 6, lines 24-36) having a status line (i.e., RQA and RQB in Fig. 14), said method comprising the steps of: time-multiplexing, from one of said satellite device and said hub device (See col. 8, line 56 through col. 9, line 4), an arbitration request signal on said link bus status line (i.e., ARBITRATION 202 and REQUEST 204 in Fig. 2 on RQA and RQB in Fig. 14); detecting (i.e., sampling), at the other of said satellite device and said hub device, said arbitration request signal (See col. 9, lines 12-16 and 34-38); determining, at said satellite device and said hub device, whether control of the link bus can be transferred from a bus master (i.e., hub agent A in Fig. 13) to said device (i.e., hub agent B in Fig. 13) issuing said arbitration request (i.e., requesting ownership of hub interface; See col. 9, lines 48-50); and if it is determined that control of

said link bus can be transferred (See col. 9, lines 52-54), transferring control of said link bus from said bus master to said device issuing said arbitration request (i.e., releasing hub agent A's ownership; See step 1310 in Fig. 13 and col. 9, lines 60-61), wherein control of said link bus is granted by said first device and said hub device (See Figs. 11-13; i.e., wherein in fact that hub agent A releases hub interface to hub agent B in Fig. 13, step 1310, inherently anticipates that control of link bus is granted by said first device and said hub device).

Referring to Claim 20, Ajanovic teaches inspecting (i.e., sampling) internal arbitration state (i.e., state of hub agent) and status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16) contained on each of said satellite device and said hub device (See Fig. 14 and col. 10, lines 24+); and determining if control of said link bus can be transferred (See col. 9, lines 48-50) based on said inspected (i.e., sampled) internal arbitration state and status information (See Figs. 11 and 12; i.e., based on state of hub agent if it is active or inactive; See col. 9, lines 12-16 and 34-38).

Referring to claim 38, Ajanovic teaches said link bus (i.e., hub interfaces A, B, C and D in Fig. 1) is a source strobed bus (i.e., hub interface with source synchronous clock mode; See col. 4, lines 35-38 and col. 6, lines 24-36).

Referring to claim 51, Ajanovic discloses a processor based system (i.e., system 100 of Fig. 1) comprising: a processor (i.e., processors 102, 104, 106 and 108 in Fig. 1); a link hub (i.e., MCH 120 of Fig. 1) for a link bus (i.e., hub interfaces A, B, C and D in Fig. 1) comprising a plurality of link bus segments (i.e., HI A, HI B, HI C and HI D in Fig. 1) each coupled to said link hub (See Fig. 1), said link hub also connected to said processor (i.e., MCH 120 coupled to processors 102, 104, 106 and 108 in Fig. 1) by a first bus (i.e., processor bus 110 of Fig. 1); a satellite device (e.g., bus agents Bridge 127 or ICH 140 in Fig. 1); and one of said link bus segments (i.e., one of hub interfaces HI A, HI B, HI C and HI D in Fig. 1) being connected between said link hub and said satellite device (e.g., connected between MCH 120 and ICH 140 in Fig. 1), and comprising a link bus status line (i.e., RQA and RQB in Fig. 14) and

having a link bus protocol (i.e., PROTOCOL LAYER), wherein said satellite device multiplexes (i.e., time-multiplexing in time slice; See col. 8, line 56 through col. 9, line 4) an arbitration signal (i.e., RQA/RQB's active/inactive signal shown in Figs. 11 and 12) on said link bus status line (See Figs. 11 and 12) in accordance with said link bus protocol (See col. 5, line 65 through col. 6, line 23) to become a master of said link bus (i.e., having ownership) during transmissions to said link hub (See col. 8, lines 43-55) and said link hub multiplexes another arbitration signal on said link bus status line in accordance with said link bus protocol to become a master of said link bus during transmissions to said satellite device (See col. 8, line 56 through col. 9, line 4), wherein control of said link bus is transferred from said master to a slave device (i.e., releasing hub agent A's ownership for hub agent B; See step 1310 in Fig. 13 and col. 9, lines 60-61).

Referring to claim 52, Ajanovic teaches said link bus is a source strobed bus (i.e., hub interface with source synchronous clock mode; See col. 4, lines 35-38 and col. 6, lines 24-36).

Referring to claim 55, Ajanovic teaches said arbitration signals (i.e., RQA/RQB's active/inactive signals shown in Figs. 11 and 12) are time multiplexed on said link bus status line during a predetermined time window (i.e., time allotted to hub interface, viz., predetermined time slice; See col. 8, line 56 through col. 9, line 4).

Referring to claim 56, Ajanovic teaches said link bus status line (i.e., RQA and RQB in Fig. 14) is used to transmit status information (i.e., active or inactive; See Fig. 11 and col. 9, lines 12-16) between said link hub (i.e., MCH 120 of Fig. 1) and said satellite device (e.g., bus agents Bridge 127 or ICH 140 in Fig. 1).

Referring to claim 57, Ajanovic discloses a processor based system (i.e., system 100 of Fig. 1) comprising: a processor (i.e., processors 102, 104, 106 and 108 in Fig. 1); a link bus hub (i.e., MCH 120 of Fig. 1) for a link bus (i.e., hub interfaces A, B, C and D in Fig. 1) comprising a plurality of link bus segments (i.e., HI A, HI B, HI C and HI D in Fig. 1) each connected to said link bus hub (See Fig. 1), said

link bus hub also connected to said processor (i.e., MCH 120 coupled to processors 102, 104, 106 and 108 in Fig. 1) by a first bus (i.e., processor bus 110 of Fig. 1); a first device (e.g., bus agents Bridge 127 of Fig. 1); and wherein one of said link bus segments (i.e., one of hub interfaces HI A, HI B, HI C and HI D in Fig. 1) is connected between said link bus hub and said first device (e.g., connected between MCH 120 and ICH 140 in Fig. 1), comprises a source strobed command/address/data bus (i.e., hub interface with source synchronous clock mode; See Fig. 14, col. 4, lines 35-38 and col. 6, lines 24-36), two clock strobes (See col. 11, lines 55-56; e.g., 66 MHz HICLK and 100MHz HICLK) and a link bus status line (i.e., RQA and RQB in Fig. 14), and supports a link bus protocol (i.e., PROTOCOL LAYER) wherein said link bus hub and a second device (e.g., ICH 140 of Fig. 1) arbitrate control over said link bus in a decentralized manner (See col. 8, lines 43-55; i.e., the arbitration between the bus agents is not controlled by a centralized arbiter, but is performed by themselves) and in accordance with said link bus protocol such that control over said link bus is transferred from a bus master (i.e., hub agent A) to a bus slave (i.e., releasing hub agent A's ownership to hub agent B; See step 1310 in Fig. 13 and col. 9, lines 60-61) when said slave is granted control over said bus (See Figs. 11-13; i.e., wherein in fact that hub agent A releases hub interface to hub agent B in Fig. 13, step 1310, inherently anticipates that control of link bus is granted by said first device and said hub device).

Referring to claim 59, Ajanovic teaches said second device (i.e., ICH 140 of Fig. 1) is a satellite device (i.e., I/O control hub agent; See col. 2, lines 52-53).

Claim Rejections - 35 USC § 103

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 3-15, 21-23, 36, 37 and 41-50 rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic [US 6,539,444 B1] as applied to claims 1, 2, 16-20, 34, 35, 38-40, 51, 52, 55-57 and 59 above, and further in view of Frame et al. [US 5,349,690 A; hereinafter Frame].

Referring to claims 3 and 36, Ajanovic discloses all the limitations of the claims 3 and 36, respectively, except that does not expressly teach said internal arbitration state information comprising a current arbitration state selected from one of a park state indicating that there are no requests on said link bus, grant-self state indicating that a device in control of said link bus is transferring information on said link bus, and a grant-other state indicating that another device is in control of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal arbitration state information comprises a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on a link bus (See col. 3, lines 28-31), grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claims 4 and 37, Ajanovic discloses all the limitations of the claims 4 and 37, respectively, except that does not expressly teach said internal status information comprising a current status value selected from one of a bus master arbitration request, bus master transfer in progress, bus slave arbitration request, and bus slave transfer in progress.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (i.e., arbitration request at t_2 after transfer completion at t_1; See col. 3, lines 45-47), bus master transfer in

progress (i.e., reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1; See col. 3, lines 54-66), bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes 12 and 16 in Fig. 1 via enabled path 42 of Fig. 2; See col. 3, lines 36-53), and bus slave transfer in progress (i.e., selected arbitration request at t_1 and transfer phase at t_1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claims 5 and 41, Ajanovic discloses all the limitations of the claims 4 and 37, respectively, except that does not expressly teach said transferring step comprising modifying internal arbitration state and status information to reflect that said issuing device is a master of said link bus and that the other device connected to said link bus is a slave of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an transferring step comprising modifying internal arbitration state and status information (i.e., modifying arbitration phases, such that wait phase 48, selection phases 50, transfer phase 52, etc in Fig. 2) to reflect that said issuing device is a master of said link bus (i.e., winning node to control the bus) and that the other device connected to said link bus is a slave of said link bus (i.e., losing node not to control the bus; See col. 3, lines 21+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claims 6 and 42, Frame teaches said internal arbitration state information comprising a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on said link bus (See col. 3, lines 28-31), grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Referring to claims 7 and 43, Frame teaches said modifying step comprising at said first device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claims 8 and 44, Frame teaches said modifying step comprising at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said first device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 9, Frame teaches said modifying step comprising at said first device (i.e., node 12 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claims 10 and 45, Frame teaches said internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (e.g., arbitration request from enabled message node 14 and 16 in Fig. 1 via enabled path 42 of Fig. 2, i.e., enabled arbitration status; See col. 3, lines 1-3), bus master transfer in progress (i.e., transfer phase 52

after the node is selected as an arbitration winner), bus slave arbitration request (e.g., path 44 of Fig. 2 for disabled message node 12 in Fig. 1, i.e., disabled arbitration status; See col. 3, lines 5-8), and bus slave transfer in progress (i.e., wait phase 48 after the node is lost the bus control; a data transfer on the bus is controlled by another node).

Referring to claims 11 and 46, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus master arbitration request (i.e., an arbitration request at t_2 after transfer completion at t_1) and not said bus slave arbitration request (i.e., not an arbitration request at t_1 from enabled message nodes). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said park state to said grant-other state if said internal status reflects said bus master arbitration request and not said bus slave arbitration request.

Referring to claims 12 and 47, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes, and the highest priority node wins to control the bus; See col. 3, lines 42-45).

Referring to claims 13 and 48, Frame teaches said internal arbitration state is changed from said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes) and not said bus slave transfer in progress state (i.e., after completion the bus slave transfer in progress state, caused by a selected arbitration request at t_1 and transfer phase at t_1). Refer to col. 3, lines 45-47.

Referring to claims 14 and 49, Frame teaches said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., an arbitration request at t_1 from enabled message nodes, which has been waiting in wait phase 48 in Fig. 2) and not said bus master transfer in progress state (i.e., after completion the transfer phase at t_2, caused by a reselected arbitration request at t_2 after transfer completion at t_1). See Fig. 2 and col. 3, lines 21+ for the operation of the fair arbitration scheme.

Referring to claims 15 and 50, Frame teaches said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said park state (i.e., bus idle state 40 in Fig. 2) if said internal status does not reflect said bus master arbitration request (i.e., no arbitration request at t_2 after transfer completion at t_1), said bus slave arbitration request (i.e., no arbitration request at t_1 from enabled message nodes) and said bus master transfer in progress state (i.e., no reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if said internal status does not reflect said bus master arbitration request, said bus slave arbitration request and said bus master transfer in progress state, i.e., said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if the bus is not busy.

Referring to claim 21, Ajanovic discloses all the limitations of the claim 21 except that does not expressly teach said internal arbitration state information comprising a current arbitration state selected from one of a park state indicating that there are no requests on said link bus, grant-self state indicating

that a device in control of said link bus is transferring information on said link bus, and a grant-other state indicating that another device is in control of said link bus.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal arbitration state information comprises a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in Fig. 2) indicating that there are no requests on said link bus (See col. 3, lines 28-31), grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) indicating that a device (i.e., node) in control of said link bus is transferring information on said link bus, and a grant-other state (i.e., wait phase 48 in Fig. 2) indicating that another device is in control of said link bus (i.e., the current node loses the control of the bus, the another node wins the control of the bus; See col. 2, lines 45-68).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 22, Ajanovic discloses all the limitations of the claim 22 except that does not expressly teach said internal status information comprising a current status value selected from one of a bus master arbitration request, bus master transfer in progress, bus slave arbitration request, and bus slave transfer in progress.

Frame discloses a fair arbitration scheme (See Abstract), wherein an internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (i.e., arbitration request at t_2 after transfer completion at t_1; See col. 3, lines 45-47), bus master transfer in progress (i.e., reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1; See col. 3, lines 54-66), bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes

12 and 16 in Fig. 1 via enabled path 42 of Fig. 2; See col. 3, lines 36-53), and bus slave transfer in progress (i.e., selected arbitration request at t_1 and transfer phase at t_1).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 23, Ajanovic discloses all the limitations of the claim 23 except that does not expressly teach said transferring step comprising modifying internal arbitration state and status information on each of said satellite device and said hub device to reflect that said issuing device is a master of said link bus and that the other device connected to said link bus is a slave of said link bus. Frame discloses a fair arbitration scheme (See Abstract), wherein an transferring step comprising modifying internal arbitration state and status information (i.e., modifying arbitration phases, such that wait phase 48, selection phases 50, transfer phase 52, etc in Fig. 2) on each of said satellite device (e.g., node 12 in Fig. 1) and said hub device (e.g., node 16 in Fig. 1) to reflect that said issuing device is a master of said link bus (i.e., winning node to control the bus) and that the other device connected to said link bus is a slave of said link bus (i.e., losing node not to control the bus; See col. 3, lines 21+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said fair arbitration scheme, as disclosed by Frame, in said method steps of said bus arbitration, as disclosed by Ajanovic, for the advantage of providing all of said devices (i.e., nodes) connected to said link bus (i.e., interconnected bus) have an equal opportunity to use said bus, but without inefficiencies created by reserving time for each device to use said bus (See Frame, col. 1, lines 50-54).

Referring to claim 24, Frame teaches said internal arbitration state information comprising a current arbitration state (i.e., arbitration phase) selected from one of a park state (i.e., bus idle state 40 in

Fig. 2), grant- self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) and a grant-other state (i.e., wait phase 48 in Fig. 2).

Referring to claim 25, Frame teaches said modifying step comprising at said satellite device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 26, Frame teaches said modifying step comprising at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said satellite device (i.e., node 12 in Fig. 1), changing said internal arbitration state to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 27, Frame teaches said modifying step comprising at said satellite device (i.e., node 12 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2); and at said hub device (i.e., node 16 in Fig. 1), changing said internal arbitration state from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2; See col. 3, lines 21-53).

Referring to claim 28, Frame teaches said internal status information comprises a current status value (i.e., current status of node) selected from one of a bus master arbitration request (e.g., arbitration request from enabled message node 14 and 16 in Fig. 1 via enabled path 42 of Fig. 2, i.e., enabled arbitration status; See col. 3, lines 1-3), bus master transfer in progress (i.e., transfer phase 52 after the node is selected as an arbitration winner), bus slave arbitration request (e.g., path 44 of Fig. 2 for disabled message node 12 in Fig. 1, i.e., disabled arbitration status; See col. 3, lines 5-8), and bus slave transfer in progress (i.e., wait phase 48 after the node is lost the bus control; a data transfer on the bus is controlled by another node).

Referring to claim 29, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus master arbitration request (i.e., an arbitration request at t_2 after transfer completion at t_1) and not said bus slave arbitration request (i.e., not an arbitration request at t_1 from enabled message nodes). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said park state to said grant-other state if said internal status reflects said bus master arbitration request and not said bus slave arbitration request.

Referring to claim 30, Frame teaches said internal arbitration state is changed from said park state (i.e., bus idle state 40 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes, and the highest priority node wins to control the bus; See col. 3, lines 42-45).

Referring to claim 31, Frame teaches said internal arbitration state is changed from said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) to said grant-other state (i.e., wait phase 48 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., arbitration request at t_1 from enabled message nodes) and not said bus slave transfer in progress state (i.e., after completion the bus slave transfer in progress state, caused by a selected arbitration request at t_1 and transfer phase at t_1). Refer to col. 3, lines 45-47.

Referring to claim 32, Frame teaches said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said grant-self state (i.e., selection phase 50 and transfer phase 52 in Fig. 2) if said internal status reflects said bus slave arbitration request (i.e., an arbitration request at t_1 from enabled message nodes, which has been waiting in wait phase 48 in Fig. 2) and not said bus master transfer in progress state (i.e., after completion the transfer phase at t_2, caused by a reselected

arbitration request at t_2 after transfer completion at t_1). See Fig. 2 and col. 3, lines 21+ for the operation of the fair arbitration scheme.

Referring to claim 33, Frame teaches said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state (i.e., wait phase 48 in Fig. 2) to said park state (i.e., bus idle state 40 in Fig. 2) if said internal status does not reflect said bus master arbitration request (i.e., no arbitration request at t_2 after transfer completion at t_1), said bus slave arbitration request (i.e., no arbitration request at t_1 from enabled message nodes) and said bus master transfer in progress state (i.e., no reselected arbitration request at t_2 and transfer phase at t_2 after transfer completion at t_1). Refer to col. 3, lines 45-47, i.e., wherein in fact that after the transfer involving node 12 has been completed, it too is disabled and must wait until the bus is idle for 1600 nsec (t_2) implies that said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if said internal status does not reflect said bus master arbitration request, said bus slave arbitration request and said bus master transfer in progress state, i.e., said internal arbitration state is changed from said internal arbitration state is changed from said grant-other state to said park state if the bus is not busy.

7. Claims 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic [US 6,539,444 B1] as applied to claims 1, 2, 16-20, 34, 35, 38-40, 51, 52, 55-57 and 59 above, and further in view of Singh et al. [US 6,609,171 B1; hereinafter Singh].

Referring to claim 53 and 54, Ajanovic discloses all the limitations of the claims 53 and 54, respectively, except that does not teach said link bus is one of a quad pumped source strobed bus and a double pumped source strobed bus.

Singh discloses a multi-pumped signaling mode operation (See col. 6, lines 33+), wherein a link bus (i.e., processor bus 117 in Fig. 2) is one of a quad pumped source strobed bus (See col. 6, lines 43+) and a double pumped source strobed bus (See col. 11, lines 14+) according to a multi-pumped signaling mode (See col. 6, lines 33+).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said means for signaling multi-pumped bus (e.g., strobe generator, strobe signal lines, and multi-pumped signaling mode controller), as disclosed by Singh, on said link bus and its connected devices (i.e., bus adapter and module), as disclosed by Ajanovic, for the advantage of increasing bus throughput by operating said link bus in the multi-pumped signaling mode (See Singh, col. 2, lines 39-42).

8. Claim 58 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ajanovic [US 6,539,444 B1] as applied to claims 1, 2, 16-20, 34, 35, 38-40, 51, 52, 55-57 and 59 above, and further in view of Rosen et al. [US 6,346,828 B1; hereinafter Rosen].

Referring to claim 58, Ajanovic discloses all the limitations of the claim 58 except that does not teach said link bus status line is a tristate status line.

Rosen discloses a method and apparatus for pulsed clock tri-state control (See Abstract), wherein a link bus status line (i.e., TRI_STATE BUS 110 of Fig. 2) is a tristate status line (See col. 4, lines 15-17). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented said pulsed clock tri-state control, as disclosed by Rosen, on said link bus, as disclosed by Ajanovic, for the advantage of improving timing to ease trouble shooting, expands signal propagation time to complete data transfer over tristate bus and eliminates race conditions (See Rosen, Fig. 3 and col. 9, lines 32-41).

Response to Arguments

9. Applicant's arguments with respect to claims 1, 19, 34, 51, 57 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Baumert et al. [US 5,469,438 A] disclose method of transmitting signals in an extendible local area network.

Rothenbaum [US 6,128,743 A] discloses intelligent system and method for universal bus communication and power.

Garney et al. [US 5,890,015 A] disclose method and apparatus for implementing a wireless universal serial bus host controller by interfacing a universal serial bus hub as a universal serial bus device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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